USER'S REFERENCE MANUAL

ADIO-104

Analog and Digital I/O Module For PC/104

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Conventions and Terminology Used Throughout This Publication

Safety and Usage Conventions

NOTE: *Contains important information and useful tips that will assist in the understanding and operation of the product.*

CAUTION: *Calls attention to a procedure, practice or condition that could possibly cause personal injury or damage to equipment.*

WARNING: *Calls attention to a procedure, practice or condition that could possibly cause severe bodily injury, death or extensive equipment damage.*

Terminology

Host This is the computer or similar device into which the ADIO-104 is plugged.

Logic conditions Unless otherwise noted, logic signals are designated as TRUE (Set) and FALSE (Clear). Names with an asterisk (*) postscript are inverted or active low. Unless otherwise noted TRUE is considered logic "1" (+5vdc) and FALSE is logic "0" (0vdc).

Numbering Systems Computerized equipment often requires its numeric data to be represented in different forms depending on the audience and information being conveyed. Decimal numbers are typically used for end-user data entry and display while internally these values are converted and manipulated in native binary. Hexadecimal numbers are often used by programmers as an intermediate level between binary and decimal notations.

Base	Name	Format (MS <---> LS)
2	Binary	1011 1001
10	Decimal	185
16	Hexadecimal	0xB9 or $B9_{16}$

Multi-Byte Word Formats
Unless otherwise specified numbers or registers spanning multiple bytes are stored in "little endian" format. The first address (ADDR+0) will contain the Least Significant Byte (LSB) while the Most Significant Byte (MSB) will reside at the highest address.

ADDR+0	ADDR	ADDR+n
LSB	LS <----> MS	MSB

Introduction

The ADIO-104 is an 8-bit PC/104 compliant module designed to satisfy common analog and digital input/output requirements in a broad range of industrial and OEM applications. In many instances, the ADIO-104 will be the only peripheral module required. Standard functions include sixteen 12-bit multi-range analog inputs, eight 12-bit multi-range analog outputs, one 8-bit binary pulse accumulator, an external interrupt input, and 24 digital I/O channels. In addition, four of the digital channels offer open-drain MOSFET outputs.

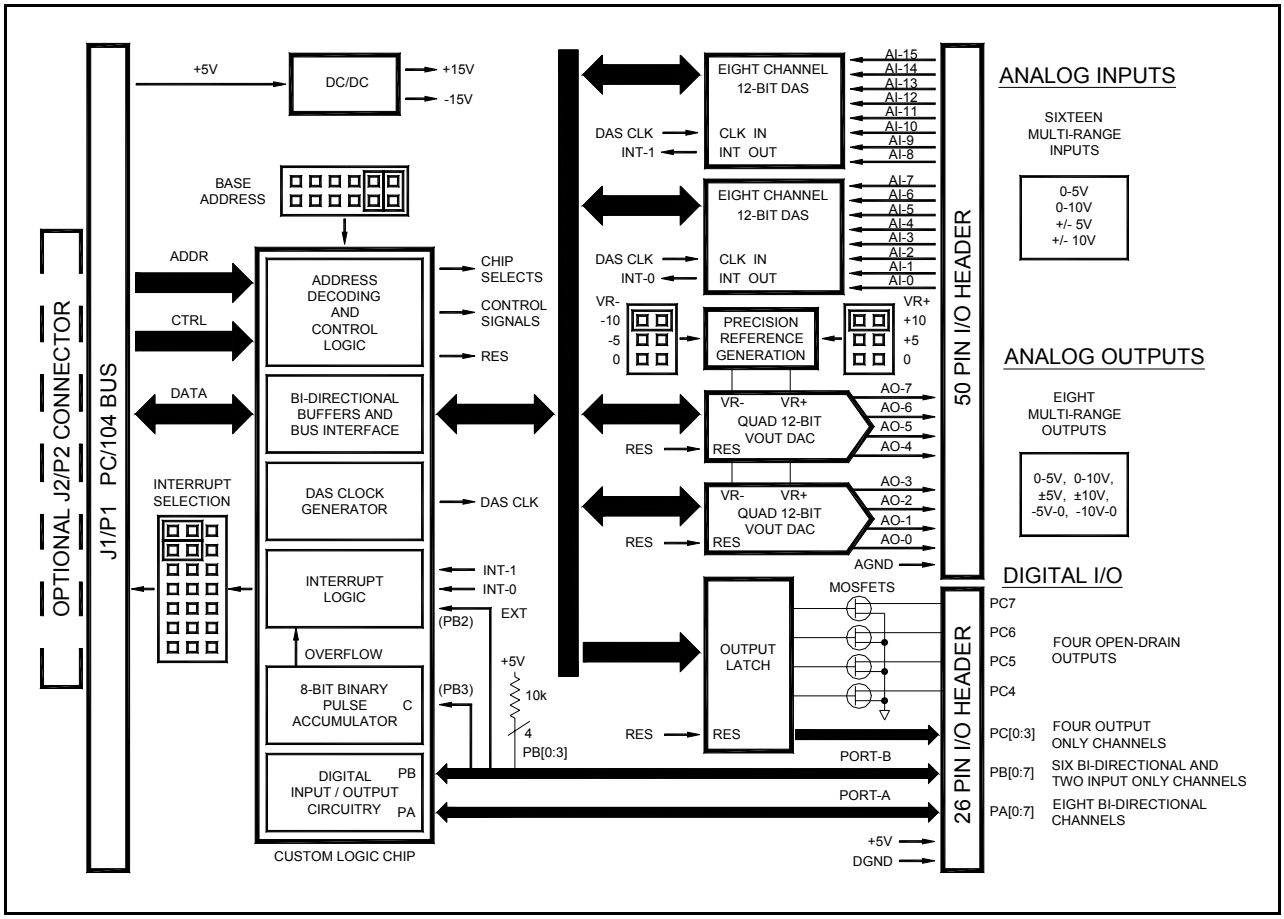


Figure 1 - ADIO Block Diagram

Component Identification

To properly apply the ADIO-104 it is necessary to become familiar with its various components. The following figure and accompanying table briefly describe their functions and locations. Subsequent sections of this manual explain their purpose and configurations in greater detail.

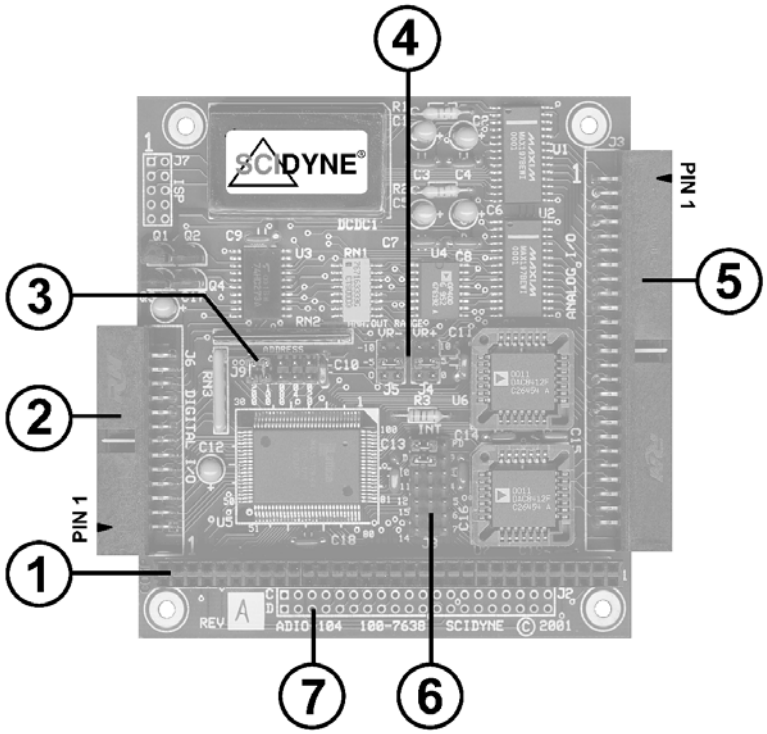


Figure 2 - ADIO-104 Component Identification

ADIO-104 Component Identification	
Item	Description
1	**PC/104 J1/P1 Connector** This connector is the 8-bit PC/104 bus.
2	**Digital I/O connector (J6)** This 26-pin IDC header is used to connect the ADIO-104 digital I/O signals to external devices. Please refer to Appendix-A for connection information.
3	**Base Address Jumpers (J9)** This jumper block determines the base address where the ADIO-104 will reside in the host's I/O map.
4	**Analog Output Range Jumpers (J4, J5,)** These jumper blocks configure the full scale output range for all of the analog outputs. J4 sets the negative reference voltage. J5 sets the positive reference voltage.
5	**Analog I/O connector (J3)** This 50-pin IDC header is used to connect the ADIO-104 analog I/O signals to external devices. Please refer to Appendix-A for connection information.
6	**Interrupt configuration jumpers (J8)** This jumper block enables and sets which interrupt request line will be used by the ADIO-104 to interrupt the host. The optional J2/P2 connector must be installed if upper interrupt request lines (IRQ10, 11, 12, 14 or 15) will be used.
7	**Optional PC/104 J2/P2 Connector** An optional 20-pin connector (J2/P2) can be installed to upgrade the ADIO-104 for 16 bit stack-through compatibility and to gain access to upper interrupt request lines.

Module Base Address and Register Map

Setting the Module Base Address

The ADIO-104 occupies 32 consecutive I/O bytes which can be set to begin on any 32-byte boundary within the host's I/O map. The factory default I/O address of 0x300 (768_{10}) is easily changed to accommodate any special requirements. The five position jumper block, J9, determines the base address. Each jumper position corresponds to a "weighted" I/O address as shown in the following table. The actual starting I/O address where the module resides is calculated by simply adding together the "weight" for each jumper that is installed.

NOTE: *Addresses between 0x000 through 0x0ff are generally used by the host and should be avoided. Make sure the I/O address selected will not conflict with any other I/O hardware.*

Example: The factory default address is set by placing jumpers in positions 0x100 and 0x200.

Installed jumper		Address value "weight"
J9-1		0x200
J9-2	+	0x100

		$0x300_{16}$ = 768_{10} = BASE ADDRESS

J9 Base Address Jumper Settings					
J9	-1	-2	-3	-4	-5
Weight (Dec)	0x200 (512)	0x100 (256)	0x080 (128)	0x040 (64)	0x020 (32)

Shaded area represents J9 factory default installed jumper positions. All other positions are left open. The values printed on the circuit board are in hexadecimal notation.

Register Map

The various ADIO-104 peripheral devices are accessed at specific offsets relative to the base address. Some of the locations are write-only, read-only or may be both written and read. Performing a read operation from a write-only location will return an indeterminate value. Writing to a read-only location will not cause a fault but should be avoided for reasons of future compatibility. Additionally, certain registers use only a few of the available data bits. When working with those registers, it is good practice to use software bit preservation techniques (AND, OR, bit-fields) so that only the meaningful bits will be examined and manipulated.

ADIO-104 I/O Register Summary

Byte Offset (dec)	Name (mnemonic)	R/W	Host Data Bus							
			D7	D6	D5	D4	D3	D2	D1	D0
0	AOCH0_LB	R/W	B7	B6	B5	B4	B3	B2	B1	B0
1	AOCH0_HB	R/W	0	0	0	0	B11	B10	B9	B8
2	AOCH1_LB	R/W	B7	B6	B5	B4	B3	B2	B1	B0
3	AOCH1_HB	R/W	0	0	0	0	B11	B10	B9	B8
4	AOCH2_LB	R/W	B7	B6	B5	B4	B3	B2	B1	B0
5	AOCH2_HB	R/W	0	0	0	0	B11	B10	B9	B8
6	AOCH3_LB	R/W	B7	B6	B5	B4	B3	B2	B1	B0
7	AOCH3_HB	R/W	0	0	0	0	B11	B10	B9	B8
8	AOCH4_LB	R/W	B7	B6	B5	B4	B3	B2	B1	B0
9	AOCH4_HB	R/W	0	0	0	0	B11	B10	B9	B8
10	AOCH5_LB	R/W	B7	B6	B5	B4	B3	B2	B1	B0
11	AOCH5_HB	R/W	0	0	0	0	B11	B10	B9	B8
12	AOCH6_LB	R/W	B7	B6	B5	B4	B3	B2	B1	B0
13	AOCH6_HB	R/W	0	0	0	0	B11	B10	B9	B8
14	AOCH7_LB	R/W	B7	B6	B5	B4	B3	B2	B1	B0
15	AOCH7_HB	R/W	0	0	0	0	B11	B10	B9	B8
16	AO_UPDATE	W	X	X	X	X	X	X	X	X
17	SIM_DAS_CTRL	W	PD1	PD0	ACQMOD		RNG	BIP	A2	A1	A0
18	DAS0_CTRL	W	PD1	PD0	ACQMOD		RNG	BIP	A2	A1	A0
	DAS0_LB	R	B7	B6	B5	B4	B3	B2	B1	B0
19	DAS0_HB	R	B11 (Bipolar, BIP=1) 0 (Unipolar, BIP=0)				B11	B10	B9	B8
20	DAS1_CTRL	W	PD1	PD0	ACQMOD		RNG	BIP	A2	A1	A0
	DAS1_LB	R	B7	B6	B5	B4	B3	B2	B1	B0
21	DAS1_HB	R	B11 (Bipolar, BIP=1) 0 (Unipolar, BIP=0)				B11	B10	B9	B8
22	PORTA	R/W	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
23	PORTB	R/W	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
24	PORTC	W	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
25	PACNT	R/W	B7	B6	B5	B4	B3	B2	B1	B0
26	INTR_STATUS	R	0	0	0	0	PAOVF	EXT	DAS1	DAS0
		W	X	X	X	X	1 = Reset PAOVF	1 = Reset EXT	X	X
27	CONFIG	R/W	PAOVF_IEN	EXT_IEN	DAS_IEN	DAS_CLK_SEL	DIR_PB_HI	DIR_PB_L0	DIR_PA_HI	DIR_PA_L0
28 - 31	Reserved	R/W	X	X	X	X	X	X	X	X

X = Don't Care

Configuration Register

The HOST application software must initialize the ADIO-104 hardware for proper operation in the intended application. This is done by writing to the configuration register which in turn sets the functionality of several ADIO-104 circuits. The **CONFIG** register is both readable and writable at anytime but is usually written only once during the application start-up sequence. All **CONFIG** register bits are automatically cleared to zero during a system power-on-reset thus creating a default state for the functions they control.

CONFIG: Configuration Register **0x1B**

	Bit 7	6	5	4	3	2	1	Bit 0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	PAOVF_IEN	EXT_IEN	DAS_IEN	DAS_CLK_SEL	DIR_PB_HI	DIR_PB_LO	DIR_PA_HI	DIR_PA_LO
Reset:	0	0	0	0	0	0	0	0

DIR_PA_LO, HI **PORTA Data Direction**

These two bits determine if the nibbles of PORTA will function as inputs or outputs.

Bit-0: DIR_PA_LO PORTA[3:0] 0 = Inputs, 1 = Outputs
Bit-1: DIR_PA_HI PORTA[7:4] 0 = Inputs, 1 = Outputs

DIR_PB_LO, HI **PORTB Data Direction**

These two bits determines if nibbles of PORTB will function as inputs or outputs.

Bit-2 DIR_PB_LO PORTB[1:0] 0 = Inputs, 1 = Outputs NOTE: PORTB[2:3] are input only
Bit-3: DIR_PB_HI PORTB[7:4] 0 = Inputs, 1 = Outputs

DAS_CLK_SEL **DAS Clock Selection**

The ADIO-104 DAS chips operate from a clock signal derived from the host bus clock. A divider is used to reduce the bus clock frequency to a range compatible with the DAS chips. Two divider values are available as determined by the state of the **DAS_CLK_SEL** bit. Please refer to the Analog Input section of this manual for a complete description of how the DAS clock selection affect data acquisition operations.

Bit-4: 0 = Bus clock / 8
1 = Bus clock / 4

DAS_IEN **DAS Interrupt Enable**

This bit enables or disables interrupts generated by the Data Acquisition System circuits

Bit-5: 0 = Disable DAS0 and DAS1 interrupts
1 = Enable DAS0 and DAS1 interrupts

EXT_IEN **EXTernal Interrupt Enable**

This bit enables or disables interrupts generated by the EXTternal digital input PORTB.2

Bit-6: 0 = Disable EXT interrupts
1 = Enable EXT interrupts

PAOVF_IEN **Pulse Accumulator Overflow Interrupt Enable**

This bit enables or disables interrupts generated by when the Pulse Accumulator overflows

Bit-7: 0 = Disable PAOVF interrupts
1 = Enable PAOVF interrupts

Analog Input / Output

The ADIO-104 provides sixteen 12-bit, single-ended, multi-range analog input channels and eight 12-bit multi-range analog output channels. All analog signals are non-isolated and share the same GND potential as the host computer. The analog I/O signals are routed to connections on the 50-position IDC header, J3, for easy external wiring. Please refer to Appendix-A to determine signal locations.

Analog Inputs

Two Maxim MAX197 chips are used to implement the sixteen analog inputs. This device is a complete multi-range DAS (Data-Acquisition-System) featuring software programmable parameters. Each channel can be individually configured to operate in one of four full-scale input ranges; ±10V, ±5V, 10V or 5V. This effectively increases dynamic range to 14-bits when employing software range-switching techniques. It also provides the flexibility to easily interface 4-20ma and bipolar sensors. Acquisition can be done automatically by the chip or under full control of the user's software. Optionally, the host can be interrupted at the end of each conversion. A special feature allows two identically configured analog input pairs to be digitized simultaneously. This capability make the ADIO-104 very useful in applications that require "Phase Coherent" data acquisition. All inputs channels are over-voltage protected to ±16.5V. This protection is active even when the ADIO-104 is not powered. Further more, an overvoltage condition on one or more channels does not affect readings taken on the remaining channels.

NOTE: *To achieve the best performance, the analog inputs should be driven from low impedance sources, ideally OP AMPS with an settling time of 1.5µs or less. Attention must also be given to maintain signal integrity by using proper shielding, wiring and grounding techniques.*

NOTE: *For simplicity in explanation and unless otherwise noted both DAS chips will be collectively identified as DASx. Where: 'x=0' refers to analog input channels 0-7 ,and 'x=1' refers to analog input channels 8-15.*

DAS Clock Selection

The DAS chips operate from a shared clock signal derived from the PC/104 bus. This clock determines the overall timing of the DAS including the aperture, acquisition and conversion intervals. Because of differences in bus speeds from various computer manufactures a divider is used to scale down the bus frequency to a value compatible with the DAS chips. By default the divider scales the bus clock by eight. However, for systems with a relatively low bus frequency the divider can be programmed to only divide by four resulting in a higher DAS clock. In all cases, the DAS clock should never exceed 2mhz for reliable operation. The divider selection is controlled by the **DAS_CLK_SEL** bit of the **CONFIG** register.

DAS Clock Frequency and (Cycle Times)		
Host Bus Frequency (MHZ)	DAS_CLK_SEL = 0 Host Bus Freq ÷ 8	DAS_CLK_SEL = 1 Host Bus Freq ÷ 4
4.77	596.250Khz (1.677µs)	1.1925Mhz (0.8386 µs)
6.00	750Khz (1.3333µs)	1.500Mhz (0.6667µs)
8.00	1.000Mhz (1.0000µs)	2.000Mhz (0.5000µs)
8.33	1.04125Mhz (0.9604µs)	2.0825Mhz (0.4802µs)
12.0	1.500Mhz (0.6667µs)	3.000Mhz (0.3333µs)

Note: Hatched areas indicate non-recommended DAS clocks.

DAS Control Register

Each analog-to-digital conversion process is started by writing to the **DASx_CTRL** register. This register is write-only and selects the analog input channel to be digitized, its range and the type of acquisition (Internal or External) to be performed. Writing to this register also clears the **DASx** flag within the **INTR_STATUS** register.

DASx_CTRL Register							
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
PD1 = 0	PD0 = 0	ACQMOD	RNG	BIP	A2	A1	A0

Bit	Name	Description
7, 6	PD1, PD0	These Bits select the clock and power-down modes. **For correct operation set Bit7 = 0 and Bit6 = 0, External clock**.
5	ACQMOD	0 = Internally controlled acquisition. 1 = Externally controlled acquisition
4	RNG	Selects the full-scale voltage at the input, 0 = 5V 1 = 10V
3	BIP	Selects unipolar or bipolar conversion mode, 0 = Unipolar 1 = Bipolar
2, 1, 0	A2, A1, A0	These are address bits for the input mux to select the "on" channel. A0 = LSB

A2	A1	A0	DAS1	DAS0	Simultaneous Pair
0	0	0	AICH8	AICH0	AICH8:AICH0
0	0	1	AICH9	AICH1	AICH9:AICH1
0	1	0	AICH10	AICH2	AICH10:AICH2
0	1	1	AICH11	AICH3	AICH11:AICH3
1	0	0	AICH12	AICH4	AICH12:AICH4
1	0	1	AICH13	AICH5	AICH13:AICH5
1	1	0	AICH14	AICH6	AICH14:AICH6
1	1	1	AICH15	AICH7	AICH15:AICH7

Internal Acquisition

Internal acquisition is the simplest mode to implement and is frequently how the analog inputs on the ADIO-104 are used. Select this mode by writing the **DASx_CTRL** register with the **ACQMOD** = 0. The desired input channel and range selection bits must also be written at this time. The write operation initiates an acquisition interval whose duration is internally timed and lasting 6 DAS clock cycles. Conversion automatically begins at the end of the acquisition interval and lasts an additional 12 DAS clock cycles. The overall start-to-finish digitization process takes 18 DAS clock cycles.

External Acquisition

Use external acquisition for precise control of the sampling aperture and/or independent control of acquisition and conversion times. The user controls acquisition and start-of-conversion with two separate write operations. The first operation, written with **ACQMOD** = 1, starts an acquisition interval of indeterminate length. The desired input channel and range selection bits are also written at this time. The second write operation, written with **ACQMOD** = 0, terminates acquisition and starts a conversion. However, if the second byte written contains **ACQMOD** = 1, another indefinite acquisition interval is started. The conversion time, once started, lasts 12 DAS clock cycles.

NOTE: *For external acquisition, the input channel and range selection bits must have the same values on the first and second write operations.*

Simultaneous Acquisition

The ADIO-104 has the ability to perform acquisition on two analog input channels simultaneously. This is accomplished by writing a DAS control byte to the **SIM_DAS_CTRL** register which in turn writes the identical information to the DAS_CTRL register of both DAS chips. The control byte follows the same rules as an individul DASx_CTRL bytes described previously. Because both DAS chips operate from the same clock source, the acquisition and conversion will be performed simultaneously. The channel selection bits (A[2:0]) determine which "pair" of channels will be used. For instance, writing a control byte with A[2:0] = "1 0 1" will select the analog input channels AICH13 and AICH5 (ie; channel '5' of both DAS chips).

Reading a Conversion

After each conversion the **DASx** flag within the **INTR_STATUS** register is set and generates an IRQ if interrupts are configured. The host can determine when a conversion is complete using three methods: by waiting longer than the overall acquisition and conversion time, by polling the **DASx** flag, or by having the **DASx** flag interrupt the host when it becomes set. Interrupts provide a high throughput potential but require more software to implement. The **DASx** flag is cleared on the first read operation or if a new **DASx_CTRL** control word is written. Another **DASx_CTRL** byte must be written to initiate the next conversion.

Since the ADIO-104 uses an 8-bit bus interface, two I/O read operations are required to access the entire 12-bit value. The output data format is binary in unipolar mode with ***1LSB = (FS / 4096)*** and twos-complement binary in bipolar mode with ***1LSB = ((2 x \|FS\|) / 4096)***. The lower eight bits (B0-B7) are stored in the first DASx I/O location. The four upper bits (B8-B11) are stored at the second DASx I/O location and appear on data bits D0-D3 respectively. The remaining four data bits (D4-D7) are either set low (in unipolar mode) or sign-extend the value of the MSB (in bipolar mode).

Analog Input Equations			
Input Range (Volts)	1_{LSB} (mv)	Vin Calculation	Value Calculation
0 to 5	1.2207mv	Vin = Value x 1.2207mv	Value = Vin / 1.2207mv
0 to 10	2.4414mv	Vin = Value x 2.4414mv	Value = Vin / 2.441mv
- 5 to + 5	2.4414mv	Vin = Value x 2.4414mv	Value = Vin / 2.4414mv
-10 to +10	4.8828mv	Vin = Value x 4.8828mv	Value = Vin / 4.8828mv

Analog Outputs

The eight analog outputs are produced by two voltage-output, quad, DAC (Digital-to-Analog Converter) chips. All outputs share a jumper-selectable range and can drive loads up to ±5mA each. A step-up DC/DC converter allows the 10V and bipolar ranges to be achieved while operating the ADIO-104 module from a single +5V supply. In addition, the DACs are double buffered. Data can be freely pre-loaded to any of the channels without immediately affecting their outputs. After each DAC to be changed is pre-loaded, writing any value to the **AO_UPDATE** register will cause the newly pre-loaded analog outputs to be updated simultaneously. The other DACs maintain their previous output voltages without interruptions or glitches. This feature is essential when using the ADIO-104 in "phase sensitive" applications such as motion control. The DACs are automatically initialized during Power-On-Reset. Depending on the model of ADIO-104 purchased, the DACs will be loaded with a zero value of 0x000 (Model RZ) or a mid-scale value of 0x800 (Model RM). The output voltage produced after Power-On-Reset depends on the output range selection.

Setting Output Range

The analog output DACs use a negative and positive reference voltage to set the minimum (when DAC value = 0x000) and maximum (when DAC value = 0xfff) voltage output swing respectively. The ADIO-104 hardware precisely generates several references voltages which are routed to two jumper blocks allowing the independent selection of the minimum and maximum output voltages. The selected output range applies to all eight analog output channels. The table shown below illustrates the possible output ranges and also indicates what the default reset output voltages will be for the two available ADIO-104 models (RM, RZ).

Analog Output Voltage Ranges			
Reference Input	Positive Reference Input DAC Value = 0xfff Jumper Block J4: VR+		
Negative Reference Input DAC Value = 0x000 Jumper Block J5: VR-	+10	+5	0
-10	-10 to +10 RM = 0.0000 RZ = -10.000	-10 to +5 RM = -2.5000 RZ = -10.000	-10 to 0 RM = -5.0000 RZ = -10.0000
-5	-5 to +10 RM = +2.5000 RZ = -5.0000	-5 to +5 RM = 0.0000 RZ = -5.0000	-5 to 0 RM = -2.5000 RZ = -5.0000
0	0 to +10 RM = +5.0000 RZ = 0.0000	-0 to +5 RM = +2.5000 RZ = 0.0000	0 to 0 RM = 0 RZ = 0

Output Transfer Function

Regardless of the range selected, the output voltage for any channel can be calculated using the following equation:

$$Vout = VR- + \frac{(|VR+| + |VR-|) \times N}{4096}$$

Where: N = *Value loaded into DAC*

The absolute magnitude that a 1_{LSB} change in a DAC value has on an analog output voltage can be determined from this equation:

$$V_{1_{LSB}} = \frac{|VR-| + |VR+|}{4096}$$

Digital Input / Output

The ADIO-104 has 24 bits of non-isolated digital I/O channels comprised of three 8-bit ports. Each port has unique capabilities as described below. All digital I/O connections are routed to a 26-pin IDC header, J6. Unless otherwise noted all channel are compatible with TTL/CMOS voltage levels. Channels configured for output operations can source or sink 5ma of current.

PORTA

PORTA is an 8-bit bidirectional port which can be freely written to and read from. The upper and lower nibbles may be individually configured for either input or output operation by setting the corresponding DIR bit within the **CONFIG** register. At reset, all channels are automatically configured for input mode (DIR = 0) and the PORTA output latch is cleared to zero.

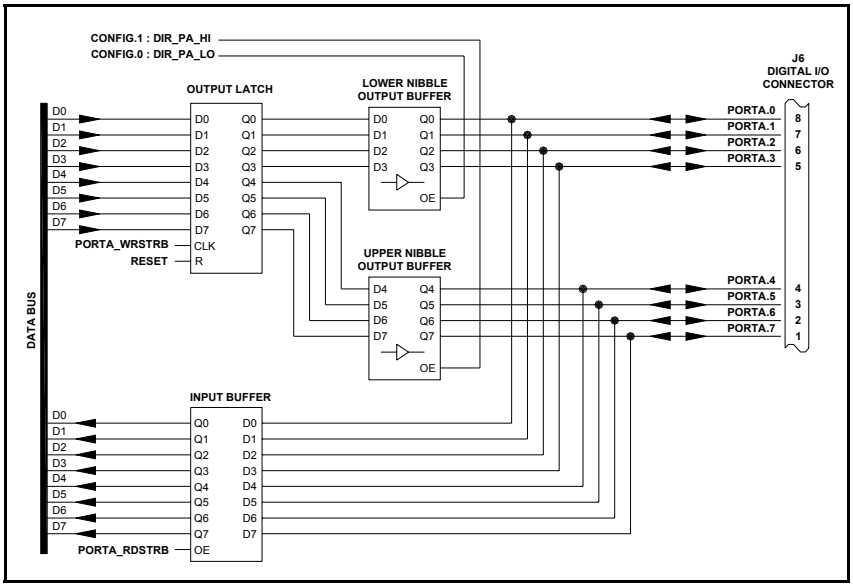


Figure 3 - PORTA Block Diagram

PORTB

PORTB is an 8-bit port. Six of the channels are bi-directional and two channels (PORTB.[2:3]) are input only. Four of the channels (PORTB.[0:3] incorporate 10k pull-up resistors simplifying their use with externally connected switches, contact closures, or open-collector devices. PORTB.2 also serves as the EXTernal interrupt input. Similarly, PORTB.3 also functions as the clock input to the Pulse Accumulator. At reset, all bi-directional channels are automatically set to input mode and the PORTB output latch is cleared to zero. To change the direction of a port nibble the corresponding DIR bit of the **CONFIG** register must be set to logic "1"

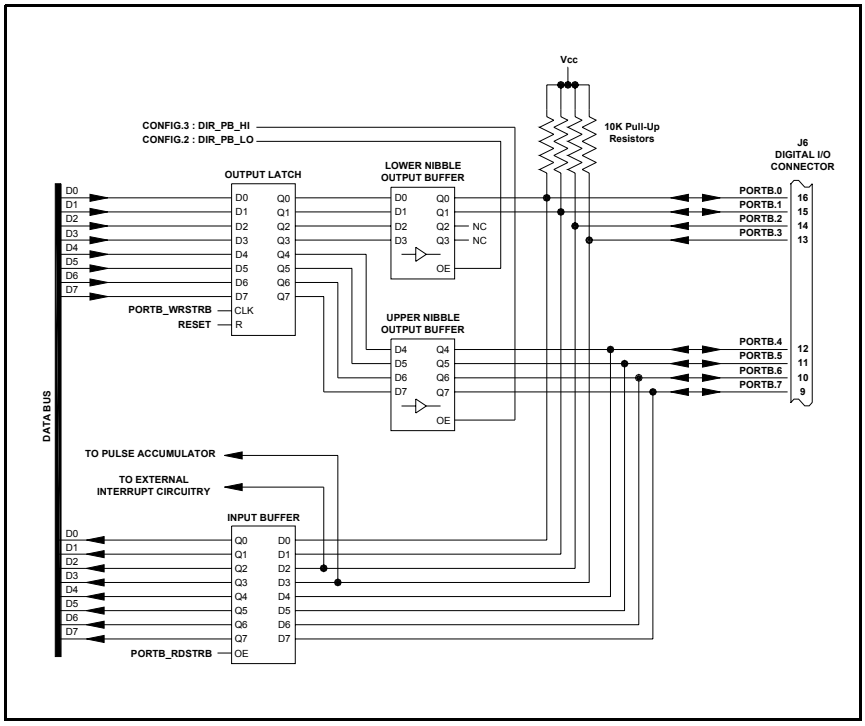


Figure 4 -PORTB Block Diagram

PORTC

PORTC is an 8-bit write only output only port. Performing a read operation will return random information. Four of the bits (PORTC.[4:7]) directly drive onboard MOSFETs providing 50V/165ma open-drain outputs. The remaining four bits (PORTC.[0:3]) can supply 25ma at TTL/CMOS voltage levels. At reset, all the open-drain outputs resort to high-impedance (Off State) while the other four bits are cleared to zero.

NOTE: *Because PORTC is write only, it is suggested that the programmer maintain a "shadow register" of PORTC in the application software. All operations destined for PORTC should be done on the shadow register prior to writing a copy of the image to the actual PORTC .*

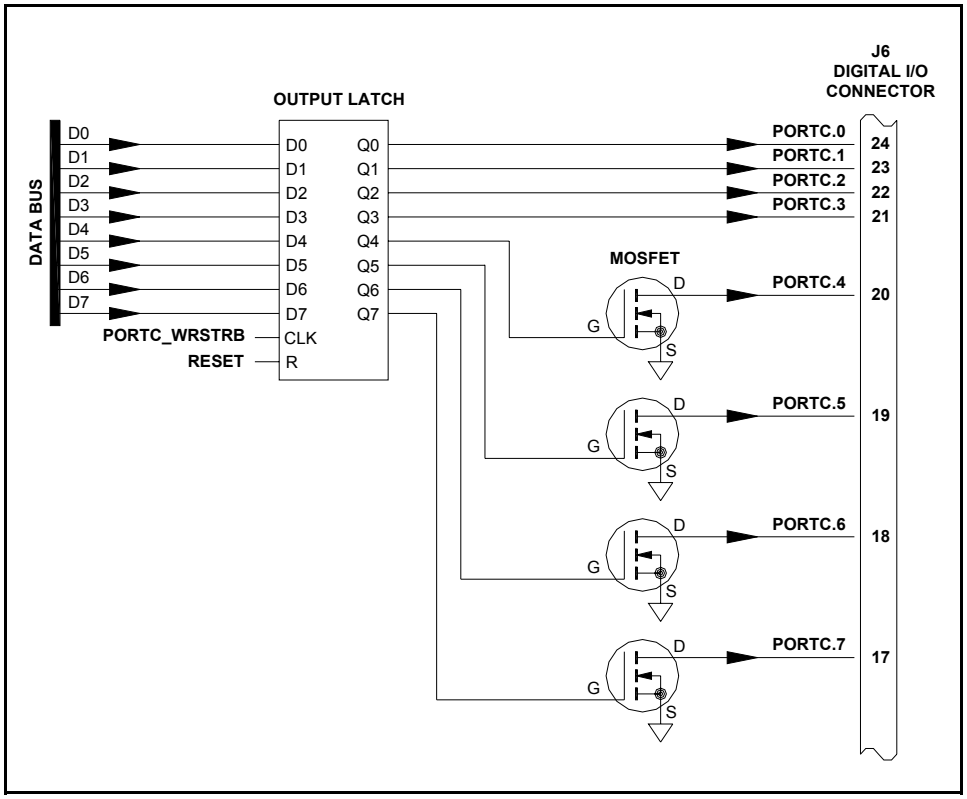


Figure 5 - PORTC Block Diagram

External Output Driver Circuits

Devices such as electro-mechanical relays generally operate at higher currents and/or voltages than can be supplied by the TTL/CMOS ADIO-104 digital outputs. If additional drive capability is required, circuits like those shown can be used.

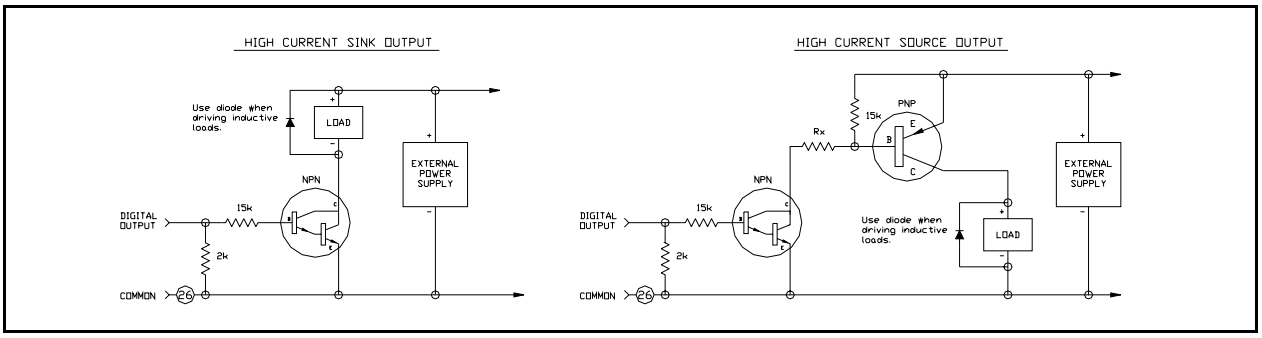


Figure 6 - External Output Driver Circuits

Over-Voltage Input Protection

The ADIO-104 digital inputs are designed to be compatible with and connect to other TTL/CMOS level signals. In some cases it may be necessary to connect to voltages much higher than the digital inputs could normally withstand. The best solution is to use optical isolation, but this is not always practical or cost-effective. An inexpensive alternative is shown. Two switching diodes and a resistor form a simple input protection circuit. Both diodes are off whenever the input signal is within the normal TTL/CMOS range. Input signals above +5.6V will forward bias D1 and clamp the digital input to one diode drop above Vcc. If the input drops below ground by more than -0.6V then D2 conducts clamping the digital input to one diode drop below ground. In either condition the excess input voltage will appear across the resistor which limits the input current to a safe level. With the values shown, inputs of ±30V are easily handled. Each digital input to be connected to a high voltage must have its own protection circuit.

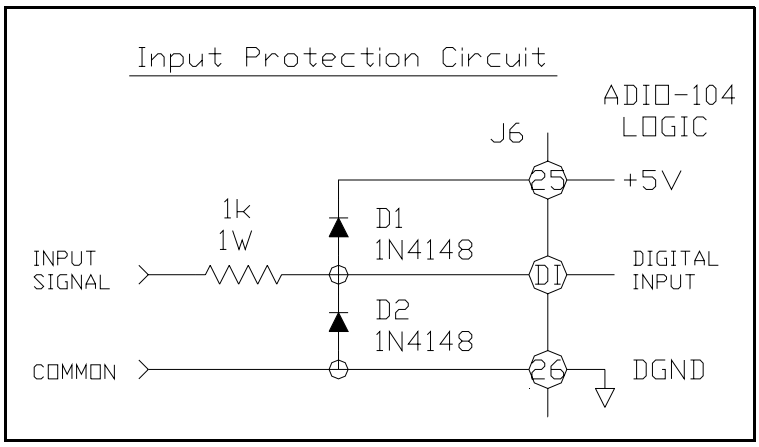


Figure 7 - Input Protection Circuit

Pulse Accumulator

An 8-bit binary pulse accumulator is provided for counting externally generated events. It can be freely written or read at any time and is automatically cleared to zero at power-on reset. The pulse accumulator count input is shared with the input-only PORTB.3 signal. Digital filtering circuitry is included to help reduce false counts created by spurious noise spikes occurring on the clock input signal. However, as a consequence, the filtering limits the maximum count rate to 250khz. For the most reliable operation it is suggested that the clock input signal be clean and have sharp rising and falling edges. Counts are incremented on the positive going edge. When the pulse accumulator rolls over from its maximum count to zero (0xFF.. 0x00) an overflow is condition is generated and recorded by setting a flip/flop whose output is the **PAOVF** flag within the **INTR_STATUS** register. The host software can examine the **PAOVF** flag at anytime to determine if an overflow has occurred. Optionally an interrupt request can be sent to the host computer whenever **PAOVF** becomes set by enabling **PAOVF_IEN** (CONFIG.7 = "1"). The **PAOVF** flag must be manually cleared by writing to the **INTR_STATUS** register with a value having **PAOVF** = "1" (0x08). The write operation resets the flip/flop and does not affect the other bits of the **INTR_STATUS** register. Failure to clear the **PAOVF** flag before another overflow occurs will result in lost overflow count information.

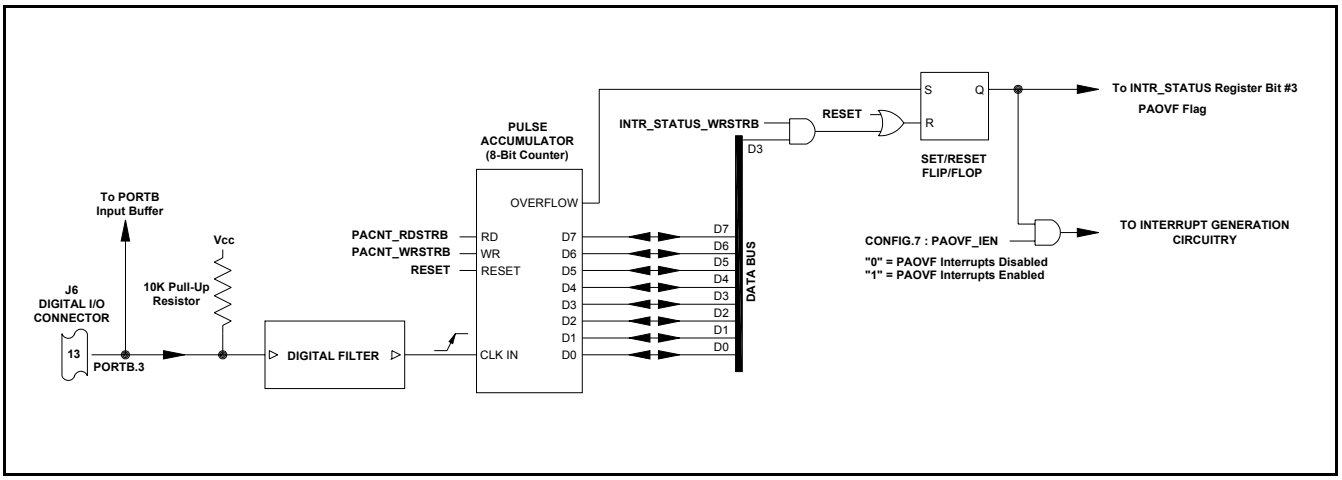


Figure 8 - Pulse Accumulator Block Diagram

Extending Counting Range

The **PAOVF** flag is commonly used to extend the count range of the pulse accumulator. The host software creates a software counter to keep track of the number of times the **PAOVF** flag has been set. Each occurrence is equal to 256 input clock cycles. To determine the overall number of input clock cycles the software counter value (multiplied by 256) is added to the value contained in the pulse accumulator.

Pre-Determined Counting

An alternative use of the **PAOVF** flag is to use it to alert the host after a certain number of events has occurred. This has an advantage in that the host does not need to constantly monitor the pulse accumulator.

Since the **PAOVF** flag gets set during roll over the pulse accumulator can be pre-set with a value equal to the 256 minus the desired value. For example, suppose an application requires that 84 events be counted. The pulse accumulator would be pre-set with a value of 172 (256 less 84). In operation, the first event would increment the pulse accumulator count to 173. The next event would increment the count to 174, and so on. After the 84th event the pulse accumulator rolls over generating an overflow which sets the **PAOVF** flag alerting the host.

Host Interrupts

Interrupt Sources and Architecture

When properly configured the ADIO-104 will generate host interrupts to signal three separate hardware events: the completion of analog-to-digital conversions, that the Pulse Accumulator has overflowed, or when a negative transition has occurred on the external digital interrupt input. Using interrupts can improve overall application performance but requires additional software and are generally more difficult to implement. These three sources share the same interrupt request channel to the host. The application software can determine the origin of the request by examining the **INTR_STATUS** register. A logic "1" in the **DAS0**, **DAS1**, **EXT** or **PAOVF** locations indicates that the corresponding hardware requires service. The remaining four bits (B<4-7>) will return logic "0". The status bits are always available and can be used for simple polling purposes even if interrupts will not be used.

Three bits within the **CONFIG** register are used to selectively configure which of the sources can generate interrupts. A logic "1" in the corresponding interrupt enable (IEN) bit will enable interrupts generated by that source. Similarly, a logic "0" will mask interrupts generated by that source.

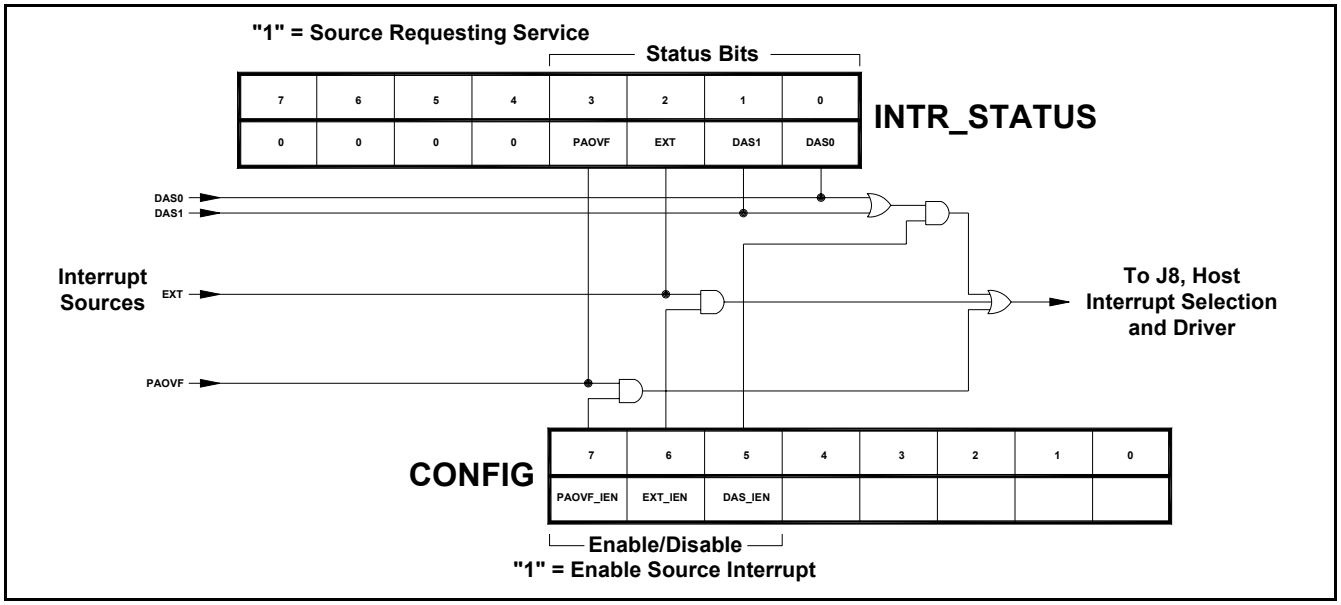


Figure 9 - ADIO-104 Interrupt Architecture

Analog-To-Digital Converters (DAS0, DAS1)

The analog-to-digital converters sets their corresponding **DAS** flag after each conversion. The flag is cleared by reading the conversion result, by writing a new control word to the corresponding **DAS_CTRL** register, or by writing to the **SIM_DAS_CTRL** register. The **DAS_IEN** bit of the **CONFIG** register must be set to "1" for DAS interrupts to be generated to the host.

External Interrupt (EXT)

The external interrupt input is shared with digital input PORTB.2. A negative going transition (from logic "1" to logic "0") will clock and set a flop/flop. The transition is remembered even if the input signal returns to logic "1" before the event is recognized by the application software. The **EXT** bit of the **INTR_STATUS** register reflects the state of the flip/flop and optionally generates a host IRQ if enabled (**CONFIG.6 EXT_IEN** = "1"). The **EXT** flip/flop must be manually cleared by writing to the **INTR_STATUS** register with a value having **EXT** = "1" (0x04). The other bits of the **INTR_STATUS** register are not affected by the write operation. Failure to clear the **EXT** flag before another PORTB.2 negative transition occurs will result in lost negative transition detection. If the external interrupt feature is not required, external interrupts should not be enabled (**CONFIG.6 EXT_IEN** = "0") and the flip/flop state can simply be ignored.

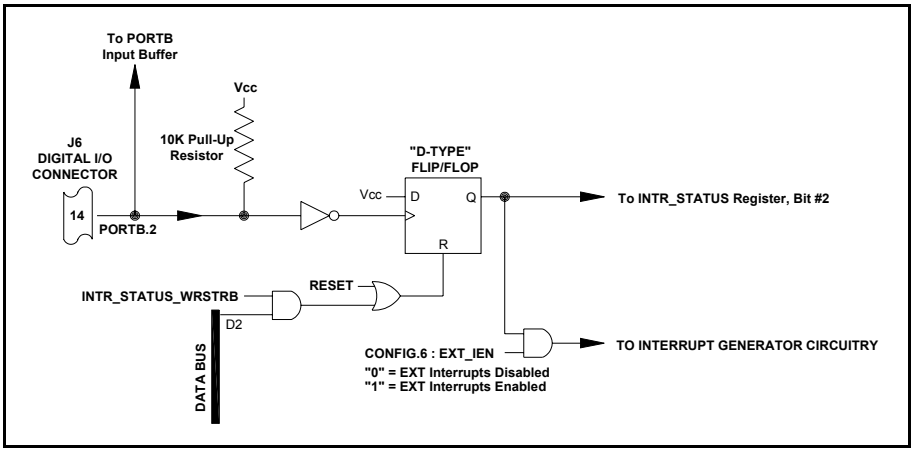


Figure 10 - External Interrupt Circuitry Block Diagram

Pulse Accumulator Overflow (PAOVF)

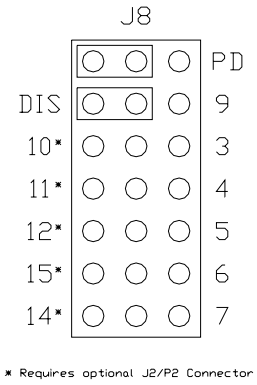
When the pulse accumulator rolls over from its maximum count to zero (0xFF.. 0x00) an overflow is generated and recorded by the setting of the **PAOVF** flag within the **INTR_STATUS** register. The host software can examine the **PAOVF** flag at anytime to determine if an overflow has occurred. Optionally an interrupt can be generated to the host computer when **PAOVF** becomes set (**PAOVF_IEN** = "1"). The **PAOVF** flag must be manually cleared by writing to the **INTR_STATUS** register with a value having **PAOVF** = 1 (0x08). The other bits of the **INTR_STATUS** register are not affected by the write operation. Failure to clear the **PAOVF** flag before another overflow occurs will result in lost overflow count information.

Host Hardware Interrupt Selection

Jumper block J8 configures which host interrupt will be associated with the ADIO-104. All host interrupts are supported, but the optional J2/P2 connector will be required to access the upper interrupt requests (IRQ10, 11, 12, 14 or 15). An interrupt is selected by placing a shorting jumper between the center row of J8 and the corresponding interrupt pin. Interrupt capability is disabled by placing a shorting jumper at the DIS position. The interrupt driver on the ADIO-104 conforms to the method for interrupt sharing as outlined in the PC/104 specification. This method recommends that one of the PC/104 modules sharing an IRQ provide a passive pull-down resistor to ground. The ADIO-104 can supply the pull-down resistor when a shorting jumper is installed at the PD position of J9. The pull-down resistor has no effect when interrupts are disabled.

NOTE: *Try selecting an interrupt which is not currently being used by other system resources. Certain interrupts have a defacto standard usage and should be avoided. If interrupts must be shared, make sure all the software applications and hardware involved support interrupt sharing. To prevent excessive current draw and the possibility of erroneous operation, use only one pull-down per IRQ.*

IRQ9 is re-directed to IRQ2 on most AT style computers.



Appendix - A J3 and J6, Input/Output Header Connections

J6 Digital I/O Header Connections			
Signal	Pin		Signal
PORTA.7	▼ 1	2	PORTA.6
PORTA.5	3	4	PORTA.4
PORTA.3	5	6	PORTA.2
PORTA.1	7	8	PORTA.0
PORTB.7	9	10	PORTB.6
PORTB.5	11	12	PORTB.4
PORTB.3 (3,4,5)	13	14	PORTB.2 (3,4,6)
PORTB.1 (3)	15	16	PORTB.0 (3)
PORTC.7 (1,2)	17	18	PORTC.6 (1,2)
PORTC.5 (1,2)	19	20	PORTC.4 (1,2)
PORTC.3 (1)	21	22	PORTC.2 (1)
PORTC.1 (1)	23	24	PORTC.0 (1)
+5V (Unfused) (7)	25	26	Digital Ground

Notes for Digital Input/Output signals
1: These channels are output only.
2: These channels are open-drain MOSFETs.
3: These channels have 10k pull-up resistors to +5V.
4: These channels are input only.
5: Pulse Accumulator clock input.
6: EXTernal interrupt input.
7: Unfused, Non-Isolated, and provided by the host computer.

J3 Analog I/O Header Connections			
Signal	Pin		Signal
Analog Ground	▼ 1	2	AICH15
Analog Ground	3	4	AICH14
Analog Ground	5	6	AICH13
Analog Ground	7	8	AICH12
Analog Ground	9	10	AICH11
Analog Ground	11	12	AICH10
Analog Ground	13	14	AICH9
Analog Ground	15	16	AICH8
Analog Ground	17	18	AICH7
Analog Ground	19	20	AICH6
Analog Ground	21	22	AICH5
Analog Ground	23	24	AICH4
Analog Ground	25	26	AICH3
Analog Ground	27	28	AICH2
Analog Ground	29	30	AICH1
Analog Ground	31	32	AICH0
Analog Ground	33	34	AOCH7
Analog Ground	35	36	AOCH6
Analog Ground	37	38	AOCH5
Analog Ground	39	40	AOCH4
Analog Ground	41	42	AOCH3
Analog Ground	43	44	AOCH2
Analog Ground	45	46	AOCH1
Analog Ground	47	48	AOCH0
Analog Ground	49	50	N.C.

Appendix - B Specifications

Analog Inputs:

General:	Two MAX197 DAS chips provides sixteen multi-range single-ended analog input channels
A/D resolution:	12-bit (1 in 4096 of full-scale), 14-bit effective dynamic range using software range-switching techniques
Input ranges:	Each channel has software programmable input range: ±10V, ±5V, +5V or +10V
Input current:	Unipolar: 750µA max., Bipolar: 1200µA max.
Overvoltage:	±16.5V protection. A fault condition on any channel will not affect readings on other channels
Nonlinearity:	±1LSB
Sampling:	50,000 samples/sec max. (Host dependent), self-timed or user controlled acquisition. Capable of simultaneous sampling on identically configured pairs; AICH0:AICH8, AICH1:AICH9 and so on.

Analog Outputs:

General:	Two DAC8412/DAC7724 chips provide eight multi-range analog output channels. Simultaneous updates
D/A resolution:	12-bit (1 in 4096 of full scale)
Output ranges:	Jumper selectable output range: +5V, +10V, -5V, -10V, ±5V or ±10V
Reset state:	Depends on model purchased. RZ = DACs set to zero ($0x000_{16}$), RM = DACs set to mid scale ($0x800_{16}$)
Output current:	±5mA max. per output
Settling time:	10µs max. to within ±½LSB of final value
Rel. accuracy:	±1LSB
Nonlinearity:	Less than ±1LSB, guaranteed monotonic

Digital I/O:

General: 24 digital I/O channels across three 8-bit ports. Unless specified otherwise all ports meet TTL/CMOS signal levels. PORTA is bi-directional. PORTB has six bi-directional channels and two input only channels functionally shared with the Pulse accumulator and External Interrupt. PORTB[0:3] feature 10k pull-up resistors. PORTC is output only. PORTC[4:7] are 50V/165ma open-drain MOSFETs.

Pulse Accumulator: Presetable 8-bit binary up counter. Clock input is shared with PORTB.3 and is positive edge sensitive. Overflows are recorded and can optionally generate interrupts. 250khz maximum count rate.

External Interrupt: Input is shared with PORTB.2. Negative edge sensitive. Transitions are recorded and can optionally generate interrupts.

Addressing: 8-bit PC/104 bus. Can be jumpered for any 32 byte block in hosts I/O map, $0x000_{16}$ through $0x3E0_{16}$

Interrupt: Optionally uses one interrupt, Jumper selectable IRQ 3, 4, 5, 6, 7, 9, (10, 11, 12, 14, 15)* or Disable. Supports interrupt sharing with other PC/104 modules. Maskable sources: Analog input DAS chips, Pulse Accumulator, and External Interrupt. *Requires optional J2/P2 stack-through connector.

Power: +5Vdc ±5% @ 340mA typical. User circuitry excluded

Dimensions: PC/104 compliant, 3.55"W x 3.775"L. 8-bit stack-through, optional 16-bit stack-through

Environmental: Operating temperature: 0C to 65C (Standard) Non-condensing relative humidity: 5% to 95%