USER'S REFERENCE MANUAL

DIO96-104

High-Density Digital Input/Output PC/104 Module

Model No. 100-7618
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Conventions and Terminology Used Throughout This Publication

Safety and Usage Conventions

NOTE: *Contains important information and useful tips that will assist in the understanding and operation of the product.*

CAUTION: *Calls attention to a procedure, practice or condition that could possibly cause personal injury or damage to equipment.*

WARNING: *Calls attention to a procedure, practice or condition that could possibly cause severe bodily injury, death or extensive equipment damage.*

Terminology

Host This is the computer or similar device into which the DIO96-104 is plugged.

Logic conditions Unless otherwise noted, logic signals are designated as TRUE (Set) and FALSE (Clear). Names with an asterisk (*) postscript are inverted or active low. Unless otherwise noted TRUE is considered logic “1" (+5vdc) and FALSE is logic “0" (0vdc).

Numbering Systems Computerized equipment often requires its numeric data to be represented in different forms depending on the audience and information being conveyed. Decimal numbers are typically used for end-user data entry and display while internally these values are converted and manipulated in native binary. Hexadecimal numbers are often used by programmers as an intermediate level between binary and decimal notations.

Base	Name	Format (MS <---> LS)
2	Binary	1011 1001
10	Decimal	185
16	Hexadecimal	0xB9 or $B9_{16}$

Multi-Byte Word Formats

Unless otherwise specified numbers or registers spanning multiple bytes are stored in “little endian” format. The first address (ADDR+0) will contain the Least Significant Byte (LSB) while the Most Significant Byte (MSB) will reside at the highest address.

ADDR+0	ADDR	ADDR+n
LSB	LS <----> MS	MSB

Introduction

The DIO96-104 is an 8-bit high-density digital Input/Output module for the PC/104 bus. It provides 96 digital I/O channels arranged as four groups containing three 8-bit ports. Each group is controlled by a separate 82C55A integrated circuit. This industry standard device offers very flexible configuration, including software programmable port directions and strobed handshaking.

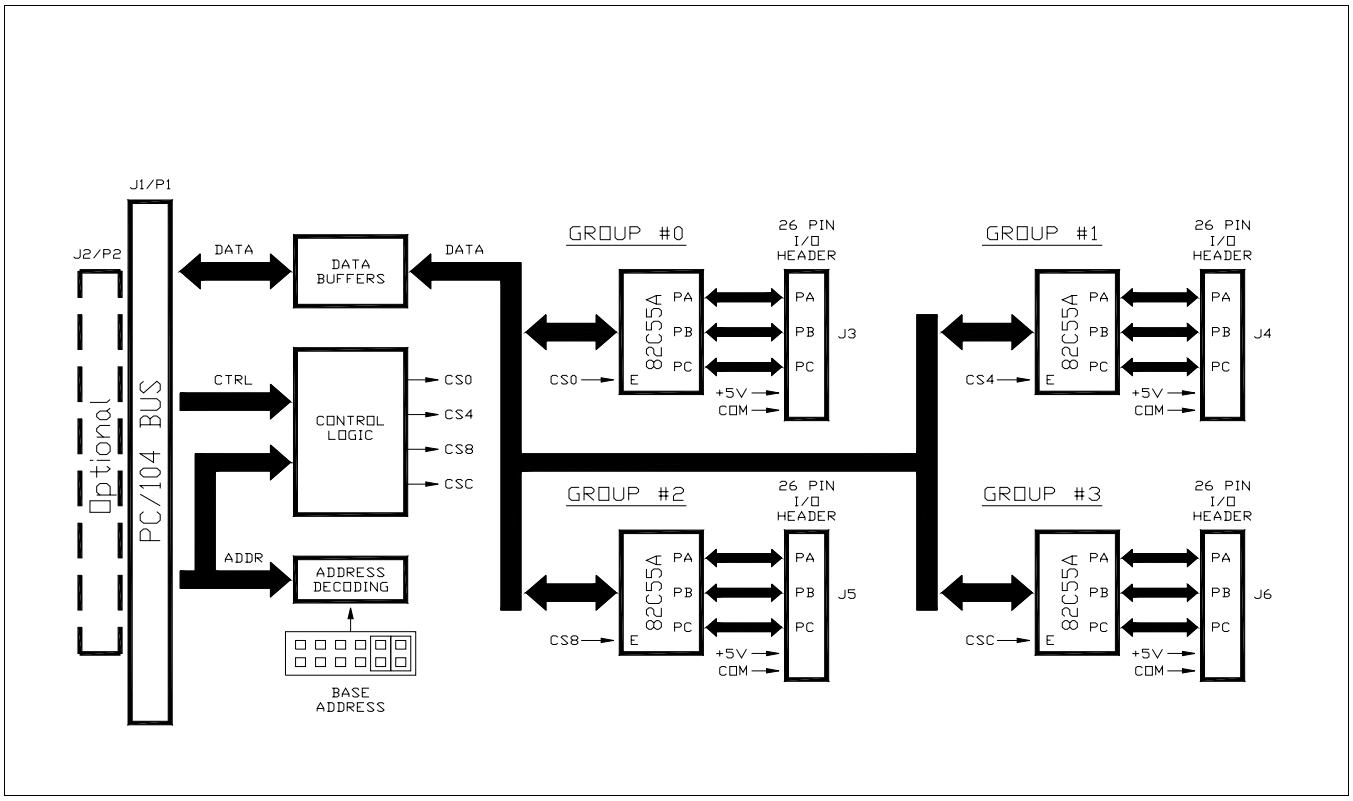

Figure 1 - DIO96-104 Block Diagram

Component Identification

Before the DIO96-104 can be put into service it must be properly configured to work in the target application. This is accomplished by correctly setting shorting jumpers on the module. The component identification is shown in Figure 2. Each DIO96-104 comes from the factory set to a basic functional default configuration. The user is free to change the default settings to satisfy any particular application requirements.

DIO96-104 Component Identification	
Item	Description
1	**PC/104 J1/P1 Connector** This connector is the 8-bit PC/104 bus.
2	**Base Address Jumpers (J7)** This jumper block determines the starting address where the module will reside in the host's I/O map.
3, 4, 5, 6	**I/O Headers (J3,J4,J5,J6)** These four 26-pin IDC headers are used to connect the DIO96-104 to external devices. Each header is associated with a particular 24-bit group and is controlled by a separate 82C55A chip. ③ = J3/Group#0, ④ = J4/Group#1, ⑤ = J5/Group#2, ⑥ = J6/Group#3
7	**Optional PC/104 J2/P2 Connector** An optional 20-pin connector (J2/P2) can be installed to upgrade the DIO96-104 for 16 bit stack-through compatibility.

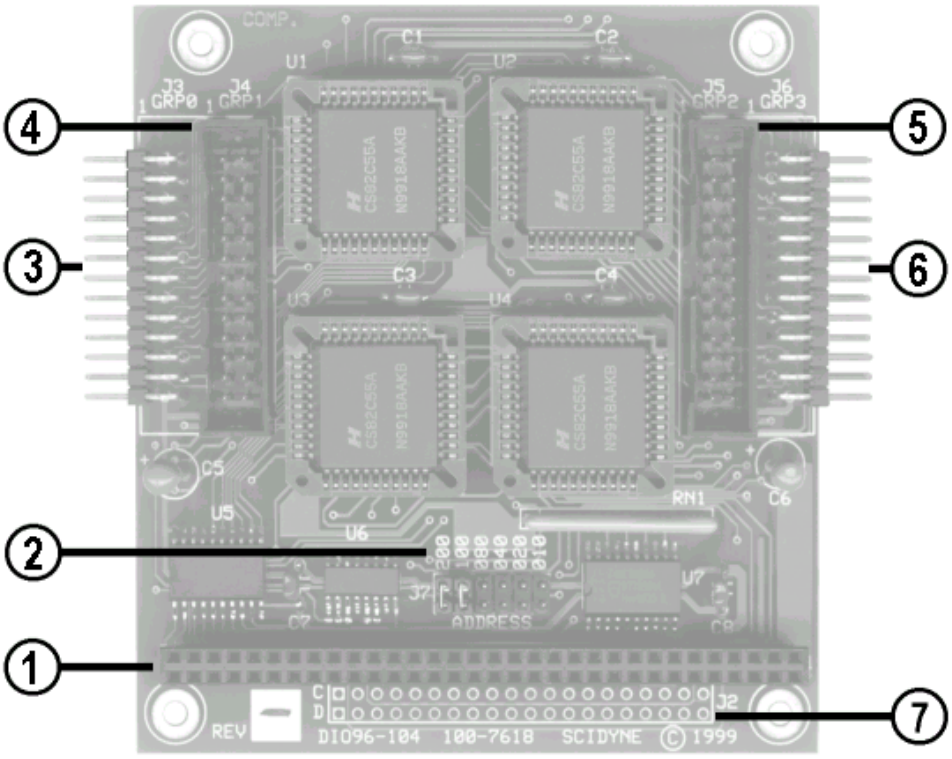

Figure 2 - DIO96-104 Component Identification

Module Base Address and Register Map

Setting the Module Base Address

The DIO96-104 occupies 16 consecutive I/O bytes and can be placed on any 16 byte boundary within the host's I/O map. The factory default I/O address is 0x300 (768_{10}) but is easily changed to accommodate any special requirements. The six position jumper block, J7, determines the base address. Each jumper position corresponds to a "weighted" I/O address as shown in the following table. The module's starting I/O address is calculated by simply adding together the "weight" for each jumper that is installed.

> NOTE: *Addresses between 0x000 through 0x0ff are generally used by the host and should be avoided. Make sure the I/O address selected will not conflict with any existing I/O hardware.*

Example: The factory default address is set by placing jumpers at positions 0x100 and 0x200.

Installed jumper	Address Value "weight"		
J7-2	0x100		(256)
J7-1	+ 0x200	+	(512)

	$0x300_{16}$	=	768_{10} = BASE ADDRESS

J7 Base Address Jumper Settings						
J7	-1	-2	-3	-4	-5	-6
Weight (Dec)	0x200 (512)	0x100 (256)	0x080 (128)	0x040 (64)	0x020 (32)	0x010 (16)

Note: Shaded areas represent J7 factory default installed jumper positions. All other positions are left open. The values printed on the circuit board are in hexadecimal notation.

Register Map

The various DIO96-104 peripheral functions are accessed at specific offsets relative to the base address. All locations are inherently readable and writeable. However, the manner in which the 82C55A chips are configured determines which locations should be treated as write-only, read-only or both written and read. Performing a read operation from a write-only location may return an indeterminate value. Writing to a read-only location will not cause a fault but should be avoided for reasons of future compatibility.

Each group is controlled by a separate 82C55A integrated circuit. This device is very versatile and has many programmable functions. The data sheet for 82C55A is not included with this manual. However, a copy is available in PDF format and can be downloaded from the SCIDYNE web site at ***www.scidyne.com***.

DIO96-104 Register Map										
Byte Offset (dec)	Name	R/W	Host Data Bus							
			D7	D6	D5	D4	D3	D2	D1	D0
J3, Group #0										
0	PORTA	R/W	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
1	PORTB	R/W	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
2	PORTC	R/W	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
3	DIO_CTRL	R/W	MODE SET FLAG	GROUP A				GROUP B		
				MODE		PA DIR	PC (HI)	MODE	PB DIR	PC (LOW)
J4, Group #1										
4	PORTA	R/W	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
5	PORTB	R/W	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
6	PORTC	R/W	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
7	DIO_CTRL	R/W	MODE SET FLAG	GROUP A				GROUP B		
				MODE		PA DIR	PC (HI)	MODE	PB DIR	PC (LOW)
J5, Group #2										
8	PORTA	R/W	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
9	PORTB	R/W	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
10	PORTC	R/W	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
11	DIO_CTRL	R/W	MODE SET FLAG	GROUP A				GROUP B		
				MODE		PA DIR	PC (HI)	MODE	PB DIR	PC (LOW)
J6, Group #3										
12	PORTA	R/W	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
13	PORTB	R/W	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
14	PORTC	R/W	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
15	DIO_CTRL	R/W	MODE SET FLAG	GROUP A				GROUP B		
				MODE		PA DIR	PC (HI)	MODE	PB DIR	PC (LOW)

Hardware Interface

General

External devices attach to the DIO96-104 through four 26-pin IDC type headers, one header for each 24-bit group. The pinout is identical for each header and is shown below.

⚠ WARNING: *Observe proper precautions when connecting to the IDC headers. Always remove power to the PC/104 computer and all external devices before connecting or de-connecting any attachments. Before re-applying power, verify that all connections made to headers are oriented correctly.*

NOTE: *A header's PIN #1 designation is printed on the circuit board and may also be identified by a small triangle molded into the connector's plastic shroud.*

Group I/O Header Associations	
Group #	IDC Connector
0	J3
1	J4
2	J5
3	J6

IDC Header Pin-Out (One header per Group)			
Pin	Description	Pin	Description
1	PA7	2	PA6
3	PA5	4	PA4
5	PA3	6	PA2
7	PA1	8	PA0
9	PB7	10	PB6
11	PB5	12	PB4
13	PB3	14	PB2
15	PB1	16	PB0
17	PC7	18	PC6
19	PC5	20	PC4
21	PC3	22	PC2
23	PC1	24	PC0
25	+5V	26	GND

Note: The +5V is supplied by the host and is not fused.

Specifications

Digital I/O:

General:	96 non-isolated digital I/O channels arranged as four 24-bit groups with each group consisting of three 8-bit ports. Each group is controlled by a separate 82C55A peripheral interface chip supporting modes 0, 1 and 2. Interrupts are not supported.
Input level:	
Low:	-0.5V min., 0.8V max
High:	2.0V min., 5.5V max.
Output level:	
Low:	0.0V min., 0.4V max.
High	3.0V min., Vcc - 0.4V max.
Current:	±2.5mA max. per channel to meet voltage level specifications

I/O connections: Four 26-position IDC type headers, one per I/O group.

Addressing: 8-bit PC/104 bus. Occupies any consecutive 16-byte block in host's I/O map, jumper selectable between 0x000 through 0x3f0

Power requirement: +5Vdc ±10% @ 7mA typical, External circuitry excluded

Dimensions: PC/104 compliant, 3.550"W x 3.775"L
8-bit stack-through, 16-bit stack-through compatible with optional J2/P2 connector

Environmental: Operating temperature: 0° to 70°C Standard. Extended temperature version available
Non-condensing relative humidity: 5% to 95%